MIZORAM PUBLIC SERVICE COMMISSION

TECHNICAL COMPETITIVE EXAMINATIONS FOR JUNIOR GRADE OF MIZORAM ENGINEERING SERVICE (M.E.S.) UNDER PUBLIC HEALTH DEPARTMENT, GOVERNMENT OF MIZORAM, MARCH, 2019.

ELECTRICAL ENGINEERING
PAPER - III

Time Allowed : 3 hours FM : 200

SECTION - A *(Multiple Choice questions)*

(100 Marks)

All questions carry equal mark of 2 each. Attempt all questions.

*This Section should be answered only on the **OMR Response Sheet** provided.*

1. An emitter in a bipolar junction transistor is doped much more heavily than the base as it increases the
(a) Emitter efficiency (b) Base transport factor
(c) Forward current gain (d) All of these

2. A zener diode works on the principle of
(a) Tunneling of charge carriers across the junction
(b) Thermionic emission
(c) Diffusion of charge carriers across the junction
(d) Hopping of charge carriers across the junction

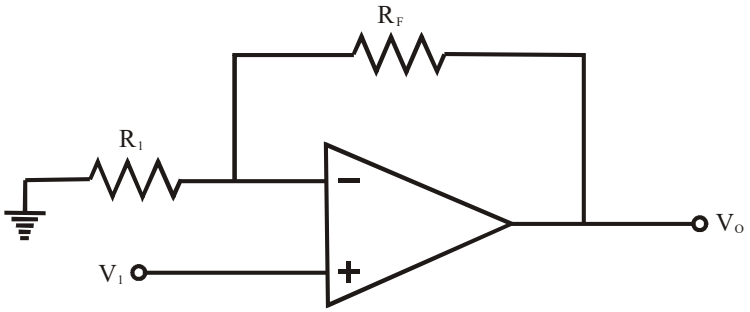
3. A long specimen of p-type semiconductor material
(a) is positively charged (b) is electrically neutral
(c) has an electrical filed directed along its length (d) acts as a dipole

4. Under small signal operation of a diode
(a) its bulk resistance increases (b) its junction resistance predominates
(c) it acts like a closed switch (d) it behaves as a clipper

5. In a multi stage R-C coupled amplifier the coupling capacitor
(a) limits the low frequency response
(b) limits the high frequency response
(c) does not affect the frequency response
(d) block the d.c. component without affecting the frequency response

6. A triangular square wave generator uses
(a) a sine wave oscillation and a comparator (b) an integrator and a comparator
(c) a differentiator and a comparator (d) a sine wave oscillator and a clipper

7. Which type of feedback is used in the following circuit

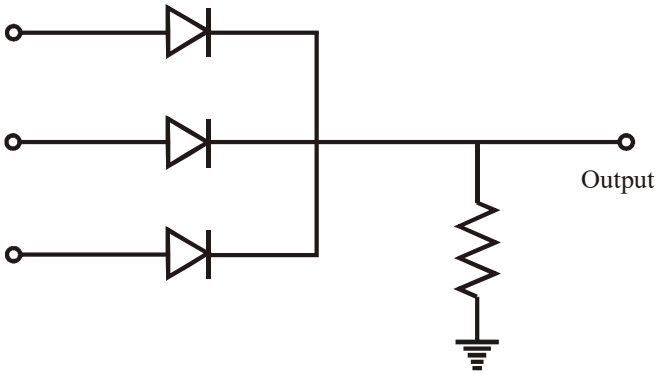


(a) Voltage series
(b) Voltage shunt
(c) Current series
(d) Current shunt

8. The race around condition exists in J-K flip flop if

(a) J=0; K=1
(b) J=1; K=0
(c) J=0; K=0
(d) J=1; K=1

9. The circuit shown in figure is 3 input gate



(a) NOR
(b) NAND
(c) OR
(d) AND

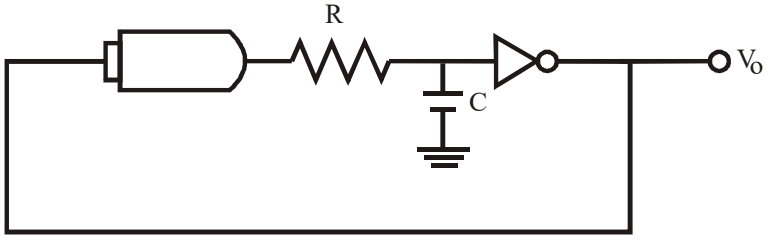
10. In Boolean algebra if $F = (A+B)(\overline{A}+C)$ then

(a) $F = AB + \overline{A}C$
(b) $F = AB + \overline{AB}$
(c) $F = AC + \overline{A}B$
(d) $F = A\overline{C} + \overline{A}B$

11. Minimum number of J-K flip-flops needed to construct a BCD counter is

(a) 2
(b) 3
(c) 4
(d) 5

12. The circuit of figure acts as



(a) Astable multivibrator
(b) Monostable multivibrator
(c) Bistable multivibrator
(d) None of these

13. Consider the following

Any combinational circuit can be built using

(1) NAND gates
(2) NOR gates
(3) EX-OR gates
(4) Multiplexers

Which of these are correct?

(a) 1, 2 and 3
(b) 1, 3 and 4
(c) 2, 3 and 4
(d) 1, 2 and 4

14. Shifting a register to the left by one bit position is equivalent to (in Binary code)

(a) Division by 2
(b) Multiplication by 2
(c) Addition of 2
(d) Subtraction of 2

15. The flip flop used in shift register are generally

(a) SR flip-flop
(b) JK flip-flop
(c) D flip-flop
(d) T flip-flop

16. In an 8085 microprocessor system with memory mapped I/O

(a) I/O devices have 16 bit addresses
(b) I/O devices are accessed using IN and OUT instruction
(c) there can be a maximum of 256 input devices and 256 output devices
(d) arithmetic and logic operations can be directly performed with the I/O data

17. The stack pointer in the 8085 microprocessor is a

(a) 16 bit register that point to stack memory locations
(b) 16 bit accumulator
(c) memory location in the stack
(d) flag register used for the stack

18. In 8085 microprocessor system, the direct addressing instruction is

(a) MOV A, B
(b) MOV B, 0AH
(c) MOV C, M
(d) STA addr

19. What is the memory word addressing capability in 8085?

(a) 32 K
(b) 64 K
(c) 256 K
(d) 512 K

20. Which one of the following is NOT a vectored interrupted?

(a) TRAP
(b) INTR
(c) RST 3
(d) RST 7.5

21. The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor

(a) 1
(b) 4
(c) 5
(d) 15

22. The synchronisation between microprocessor and memory is done by

(a) ALE signal
(b) HOLD signal
(c) READY signal
(d) None of these

23. A typical cell, for a dynamic RAM can be implemented by using how many MOS transistor?

(a) Six (b) Five

(c) One (d) Two

24. In the 8085 microprocessor, the RST6 instruction transfers the program execution to the following locations

(a) 30H (b) 24H

(c) 48H (d) 60H

25. If the accumulator of an Intel 8085 A microprocessor contains 37 H and the previous operation has set the carry flag, the instruction ACI 56 H will result in

(a) 8E H (b) 94 H

(c) 7E H (d) 84 H

26. How many times will the following loop be executed?

```
        LXI B, 0010 H
LOOP :  DCX B
        MOV A, B
        ORA C
        JNZ LOOP
```

Select the correct answer using the code given above:

(a) 10 (b) 100

(c) 16 (d) 15

27. The instruction that does not clear the accumulator of 8085 is

(a) XRA A (b) ANI 00H

(c) MVI A, 00H (d) None of these

28. Which of the following interrupts has the lowest priority?

(a) RST 5.5 (b) RST 7.5

(c) TRAP (d) INTR

29. Addition of two periodic signals will always be

(a) Periodic (b) Aperiodic

(c) May or may not be periodic (d) Insufficient data

30. In a communications system, noise is most likely to affect the signal

(a) at the transmitter (b) in the channel

(c) in the information sources (d) at the destination

31. The modulation index of an AM wave is changed from 0 to 1. The transmitted power is

(a) unchanged (b) halved

(c) doubled (d) increased by 50 percent

32. A 50.004 MHz carrier is to be frequency modulated by a 3 KHz audio tone resulting in a narrow band FM signal. Determine the bandwidth of the FM signal

(a) 2 KHz (b) 4 KHz

(c) 6 KHz (d) 4 MHz

33. Which of the following pulse modulation systems is analog?

(a) PCM (b) Differential PCM

(c) PWM (d) Delta

34. A television signal is sampled at a rate of 20% above the Nyquist rate. The signal has a bandwidth of 6 MHz. The samples are quantized into 1024 levels. The minimum bandwidth required to transmit this signal would be

(a) 72 M bits/sec (b) 144 M bits/sec

(c) 72 k bits/sec (d) 144 K bits/sec

35. If the number of bits per sample in PCM system is increased from n to n+1, then the improvement in signal to quantization noise ratio will be

(a) 3 dB (b) 6 dB

(c) 2n dB (d) 0 dB

36. The output of the vertical amplifier applied to the yoke in a TV receiver consists of

(a) direct current (b) amplified vertical sync pulses

(c) a sawtooth voltage (d) a sawtooth current

37. A superheterodyne receiver with an IF of 450 kHz is tuned to a signal at 1200 kHz. The Image frequency is

(a) 750 kHz (b) 900 kHz

(c) 1650 kHz (d) 2100 kHz

38. On increasing the number of pulse in rectification the form factor, ripple frequency and efficiency

(a) all increase

(b) decrease, decrease and increase respectively

(c) decrease, increase and increase respectively

(d) increase, decrease and increase respectively

39. A gate turn off (GTO) thyristor

(a) Requires a special turn off circuit like a thyristor

(b) Can be turned off by removing the gate pulse

(c) Can be turned off by a negative current pulse at the gate

(d) Can be turned off by a positive current pulse at the gate

40. In a three phase full wave a.c. to d.c. converter, the ratio of output ripple frequency to the supply voltage frequency is

(a) 2 (b) 3

(c) 6 (d) 12

41. In a 3 phase full converter, the output voltage during overlap is equal to

(a) Zero

(b) Source voltage

(c) Source voltage minus the inductance drop

(d) Average value of the conducting phase voltages

42. Which of the following devices should be used as a switch in a low power switched mode power supply (SMPS)?

(a) GTO (b) MOSFET

(c) TRIAC (d) THYRISTOR

43. In dc choppers, per unit ripple is maximum when duty cycle a is

(a) 0.1 (b) 0.3

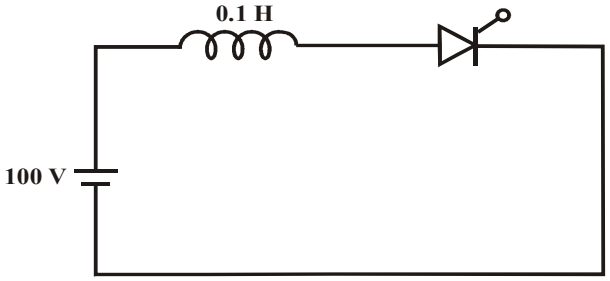
(c) 0.5 (d) 0.7

44. Which of the following characteristics are possessed by IGBT

1. High input impedance,
2. Secondary discharge problem
3. Current controlled device,
4. Low switching loss
5. Faster than BJT

(a) 1, 4 and 5 (b) 1, 2 and 4
(c) 2, 3 and 5 (d) 1, 3 and 5

45. The latching current in the given circuit is 4 mA. The minimum width of the gate pulse required to properly turn on the thyristor is



(a) 6 ms (b) 4 ms
(c) 2 ms (d) 1 ms

46. In a three phase voltage source inverter operating in square wave mode, the output line voltage is free from

(a) 3^{rd} harmonic (b) 7^{th} harmonic
(c) 11^{th} harmonic (d) 13^{th} harmonic

47. In single pulse modulation of PWM inverters, the pulse width is 120^0. For an input voltage of 220 V dc, the r.m.s value of output voltage is

(a) 179.63 V (b) 254.04 V
(c) 127.02 V (d) 185.04 V

48. A step up chopper has source voltage 50 V and output 100 V. If the pulse width is 10 μsec, the chopping frequency will be

(a) 50 KHz (b) 100 KHz
(c) 5 KHz (d) 10 KHz

49. Power electronic device with poor turn off gain is

(a) a symmetrical thyristor (b) a conventional thyristor
(c) power bipolar junction transistor (d) gate turn off thyristor

50. In a thyristor controlled reactor, the firing angle of thyristor is to be controlled in the range of

(a) 0^0 to 90^0 (b) 0^0 to 180^0
(c) 90^0 to 180^0 (d) 90^0 to 270^0

SECTION - B *(Short answer type question)*
(100 Marks)

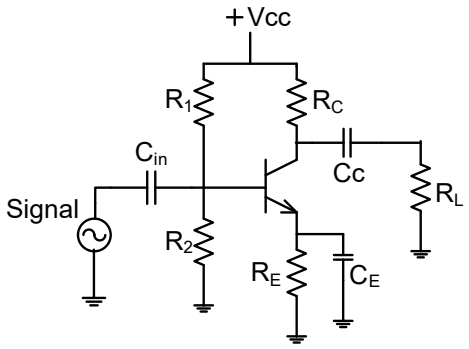
*All questions carry equal marks of **5** each.*

*This Section should be answered only on the **Answer Sheet** provided.*

1. Explain the working of a full wave bridge rectifier. What are the advantages of a bridge rectifier over a full wave rectifier?

2. Explain the phenomenon of narrowing the channel in a FET. How does this affect the flow of carriers through it?

3. In the transistor amplifier shown in figure below, R_c=10 kW, R_L=30 kW and V_{CC}=20V. The value of R_1 and R_2 are such so as to fix the operating point at 10V and 1mA. Draw the DC load line. Assume R_E to be negligible. What will be the voltage gain of the circuit if R_{in} = 1 kW and b=100?



4. Prove that both the stability and bandwidth of an amplifier increases by employing negative feedback.

5. Prove that NAND gate is the universal building block of logic gates. Illustrate your answer by making use of at least two examples.

6. Compare the Memory Mapped interfacing and I/O Mapped interfacing scheme of 8085 microprocessor.

7. Design an interface circuit for a microprocessor controlled system to meet the following:
   (a) 3-8 decoder.
   (b) EPROM (2K × 8): address range begins at 0000_H

8. Briefly explain the minimum mode and maximum mode operations in 8086 microprocessor.

9. Briefly explain the different types of addressing mode in 8085 microprocessor.

10. Draw and explain the memory write machine cycle of 8085 microprocessor.

11. Explain the difference between DSB/SC & SSB/SC modulation? Which one is advantageous and why? Which modulation procedure is followed for transmission of picture signal in TV broadcasting?

12. What is frequency modulation? 'In FM, un-modulated carrier power is equal to the total modulated signal power'- Explain.

13. What do you mean by quantization error? Deduce the relation of quantization error with step size.

14. 24 telephone channels, each band limited to 3.4 KHz, are to be time division multiplexed by using PCM. Calculate the bandwidth of PCM system for 128 quantisation levels and an 8 KHz sampling frequency.

15. Describe the different modes of operation of a thyristor with the help of its static I-V characteristics.

16. A single phase full converter is supplied from 230 V, 50 Hz source. The load consists of R = 10 ohm and a large inductance so as to render the load current constant. For a firing angle delay of 30^0, determine average output voltage and average output current and r.m.s value of thyristor current.

17. Derive an expression for the average output voltage in terms of input voltage and duty cycle of a step up chopper.

18. What is line commutated inverters? How do they operate? What is the purpose of connecting diodes in anti parallel with thyristors in inverter circuit?

19. Discuss the principles of phase control in single phase full wave ac voltage controller. Derive an expression for the r.m.s. value of its output voltage.

20. What is SMPS? Describe SMPS with a push-pull configuration.

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