## MIZORAM PUBLIC SERVICE COMMISSION

## Competitive Examinations for Junior Grade of M.E.S. under Public Works Department, August, 2018.

## ELECTRICAL ENGINEERING PAPER-III

## SECTION - A (Multiple Choice questions) <br> (100 Marks)

All questions carry equal mark of 2 each. Attempt all questions. This Section should be answered only on the OMR Response Sheet provided.

1. Diffusion of impurities in a semiconductor is carried out in a furnace through which a steady stream of impurity atoms is passed during the entire diffusion process. What would be the type of profile of the impurity atoms inside the semiconductor?
(a) Linear
(b) Gaussian
(c) Complementary error function
(d) Exponential
2. Which one of the following pairs of 8086 microprocessor's interrupt is not correctly matched?
(a) INT 0: Divide by zero
(b) INT 1: Single step
(c) INT $2:$ Break point
(d) INT 4: Overflow
3. Let $\mathrm{m}(\mathrm{t})=\cos \left[\left(2 \pi \times 10^{3}\right) \mathrm{t}\right]$ be the message signal and $\mathrm{c}(\mathrm{t})=15 \cos \left[\left(2 \pi \times 10^{6}\right) \mathrm{t}\right]$ be the carrier. $\mathrm{c}(\mathrm{t})$ and $\mathrm{m}(\mathrm{t})$ are to generate an AM signal. The modulation index of the generated AM signal is 0.5 . The ratio of the upper sideband power to the carrier power
(a) $1 / 2$
(b) $1 / 4$
(c) $1 / 8$
(d) $1 / 16$
4. The feedback diodes in a d.c. to a.c. thyristor inverter
(a) Freewheel the load current
(b) Provide reverse bias effectively to the thyristors for turn-off
(c) Improve the switching properties of the inverter
(d) Improve the harmonic distortion of the inverter output current
5. The drift velocity of electrons, in silicon
(a) is proportional to the electric filed for value of electric field.
(b) is independent of the electric field.
(c) increases at low values of electric field and decreases at high value of electric field exhibiting negative differential resistance.
(d) increases linearly with electric field at low value of electric field and gradually saturates at higher values of electric field.
6. In a 8085 microprocessor, the following sequence of instructions is executed

STC
CMC
MOV A, B
RAl
MOV B, A
After the last instruction, the output will
(a) rotate the contents of the accumulator and store it in B
(b) get the contents of B register into
(c) double contents of B register
(d) manipulate carry in A and B
7. Consider the case that noise phase modulates the FM wave. As the noise sideband frequency approaches the carrier frequency, the noise amplitude
(a) remains constant
(b) is decreased
(c) is increase
(d) is equalised
8. The 6 V zener diode shown in figure has zero zener resistance and a knee current of 5 mA . The minimum value of $R$ so that the voltage across it does not fall below 6 V is

(a) $1.2 \mathrm{~K} \Omega$
(b) $80 \Omega$
(c) $50 \Omega$
(d) $0 \Omega$
9. AC-to-DC circulating current dual converters are operated with the following relationship between their triggering angles ( $\alpha_{1}$ and $\alpha_{2}$ )
(a) $\alpha_{1}+\alpha_{2}=180^{\circ}$
(b) $\alpha_{1}+\alpha_{2}=360^{\circ}$
(c) $\alpha_{1}-\alpha_{2}=180^{\circ}$
(d) $\alpha_{1}+\alpha_{2}=90^{\circ}$
10. The contents of Register (B) and Accumulation (A) of 8085 microprocessor are 49 H and 3 AH respectively. The contents of A and the status of carry flag (CY) and sign flag (S) after executing SUB $B$ instructions are
(a) $\mathrm{A}=\mathrm{F} 1, \mathrm{CY}=1, \mathrm{~S}=1$
(b) $\mathrm{A}=0 \mathrm{~F}, \mathrm{CY}=1, \mathrm{~S}=1$
(c) $\mathrm{A}=\mathrm{F} 0, \mathrm{CY}=0, \mathrm{~S}=0$
(d) $\mathrm{A}=1 \mathrm{~F}, \mathrm{CY}=1, \mathrm{~S}=1$
11. Communication system is to be designed to provide an output SNR of 30 dB . The ratio $\frac{\mathrm{s}_{\mathrm{i}}}{2 \mathrm{Nf} f_{\mathrm{m}}}=10 \mathrm{~dB}$ is measured from bandwidth point of view which of the following modulation is preferred?
(a) FM
(b) PCM
(c) Both are having same band width
(d) None
12. An npn transistor has a beta cut off frequency $f_{\beta}$ of a 1 MHz , and a common emitter short circuit low frequency current gain $\beta$ of 200. Its unity gain frequency $f_{T}$ and the $\alpha$ cut off frequency $f_{\alpha}$ respectively are
(a) $200 \mathrm{MHz}, 201 \mathrm{MHz}$
(b) $200 \mathrm{MHz}, 199 \mathrm{MHz}$
(c) $199 \mathrm{MHz}, 200 \mathrm{MHz}$
(d) $200 \mathrm{MHz}, 200 \mathrm{MHz}$
13. In a single-phase voltage controller with RL load $\alpha$ is the firing angle $\phi$ is the load phase angle and $\beta$ is the extinction angle. For this voltage controller output power can be controlled if $\alpha>\phi$ and
(a) $(\beta-\alpha)=\pi$
(b) $(\beta-\alpha)<\pi$
(c) $\beta>\pi$
(d) Both (b) \& (c)
14. To avoid thermal runaway in the design of an Analog circuit, the operating point of BJT should be such that, it satisfies the condition
(a) $V_{C E}=\frac{1}{2} V_{C C}$
(b) $V_{C E} \leq \frac{1}{2} V_{C C}$
(c) $V_{C E} \geq \frac{1}{2} V_{C C}$
(d) $V_{C E} \leq 0.78 V_{C C}$
15. In PCM, the conditional probability of error is proportional to
(a) Noise Power $\left(\mathrm{N}_{0}\right)$
(b) Peak Signal Energy $\left(\mathrm{E}_{\max }\right)$
(c) $\sqrt{N_{0}}$
(d) $\sqrt{E_{\text {max }}}$
16. Consider the transistor circuit given below. The transistors have high values of â and a $\mathrm{V}_{\mathrm{CE}}=0.65$ Volts. The current I flowing through the $2 \mathrm{~K} \Omega$ resistance will be

(a) 1 mA
(b) 3.33 mA
(c) 0 mA
(d) 5 mA
17. Two p-n junction diodes are connected back to back to make a transistor. Which one of the following is correct?
(a) The current gain of such a transistor will be high.
(b) The current gain of such a transistor will be moderate.
(c) It cannot be used as a transistor due to large base width.
(d) It can be used only for pnp transistor.
18. If a phase controlled voltage regulator has source voltage 100 volts and $\mathrm{V}_{\text {RMS }}$ (output) is 75 volts, then input p.f. is
(a) $\frac{1}{\sqrt{\pi}}$
(b) $\frac{1}{\pi}$
(c) insufficient data
(d) None of these
19. One of the advantages of base modulation over collector modulation of a transistor class C amplifier is
(a) The lower modulating power required
(b) Higher power output per transistor
(c) Better efficiency
(d) Better linearity
20. Which one of the following statements is correct in respect of BJT?
(a) Avalanche multiplication starts when the reverse biased collector-base voltage $\mathrm{V}_{\mathrm{CB}}$ equals the avalanche breakdown voltage $\mathrm{BV}_{\text {CBо }}$.
(b) The early effect starts as soon as punch through occurs in a transistor.
(c) The small signal current gain $\mathrm{h}_{\mathrm{fe}}=$ large signal current gain $\mathrm{h}_{\mathrm{FE}}$ when $\frac{\partial h_{F E}}{\partial I_{C}}=0$.
(d) In the CE mode, a transistor can be cut off by reducing $\mathrm{I}_{\mathrm{B}}$ to zero.
21. When the gate-to-source $\left(\mathrm{V}_{\mathrm{GS}}\right)$ of a MOSFET with threshold voltage of 400 mV , working in saturation is 900 mV , the drain current is observed to be 1 mA . Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied $\mathrm{V}_{\mathrm{GS}}$ of 1400 mV is
(a) 0.5 mA
(b) 2.0 mA
(c) 3.5 mA
(d) 4.0 mA
22. In the energy band diagram of an open circuited pn junction, the energy band of n-region has shifted relative to that of p -region.
(a) downward by $\mathrm{E}_{0}$
(b) upward by $\mathrm{E}_{0}$
(c) downward by $\mathrm{E}_{0} / 2$
(d) upward by $\mathrm{E}_{0} / 2$
23. High power efficiency of the push-pull amplifier is due to the fact that
(a) each transistor conductors on different cycle of the input
(b) transistors are placed in CE configuration
(c) there is no quiescent collector current
(d) low forward biasing voltage is required
24. When RET instruction is executed by any subroutine then
(a) the top of the stack will be popped out and assigned to the PC
(b) without any operation, the calling program would resume from instruction immediately following the call instruction.
(c) the PC will be incremented after the execution of the instruction
(d) without any operation, the calling program would resume from instruction immediately following the call instruction, and also the PC will be incremented after the execution of the instruction.
25. In the case-code amplifier shown in figure, if the common-emitter stage $\left(Q_{1}\right)$ has a transconductance $\mathrm{g}_{\mathrm{m} 1}$, and the common base stage $\left(\mathrm{Q}_{2}\right)$ has a transconductance of the cascade amplifier is

(a) $\mathrm{g}_{\mathrm{m} 1}$
(b) $\mathrm{g}_{\mathrm{m} 2}$
(c) $\mathrm{g}_{\mathrm{ml}} / 2$
(d) $\mathrm{g}_{\mathrm{m} 2} / 2$
26. A two-stage amplifier is required to have an upper cut off frequency of 2 MHz and a lower cut off frequency of 30 Hz . The upper and lower cut off frequencies of individual stage are respectively
(a) $4 \mathrm{MHz}, 60 \mathrm{MHz}$
(b) $3 \mathrm{MHz}, 20 \mathrm{MHz}$
(c) $3 \mathrm{MHz}, 60 \mathrm{MHz}$
(d) $4 \mathrm{MHZ}, 20 \mathrm{MHz}$
27. During the turn-off process of a thyristor the current flow does not stop at the instant when the current reaches zero but continues to flow to a peak value in the reverse direction. This is due to
(a) commutation failure
(b) hole storage effect
(c) presence to reverse voltage across the thyristor
(d) protection inductance in series with the thyristor
28. In a bistable multivibrator, commuting capacitors are used to
(a) increase the base storage charge
(b) provide a.c. coupling
(c) increase the speed of response
(d) alter the frequency of the output
29. The memory address of the last location of a 1 K byte memory chip is given as 0 FBFFH. What will be the address of the first location
(a) 0 F 817 H
(b) 0 F 818 H
(c) 0 F 800 H
(d) 0 F 801 H
30. The voltage gains of an amplifier without feedback and with negative feedback respectively are 100 and 20. The percentage of negative feedback $(\beta)$ would be
(a) $40 \%$
(b) $50 \%$
(c) $20 \%$
(d) $80 \%$
31. A chopper oerating at a fixed frequency is feeding an RL load. As the duty ratio of the chopper is increased from $25 \%$ to $75 \%$, the ripple in the load current
(a) remains constant
(b) decreases, reaches a minimum at $50 \%$ duty ratio and then increases
(c) increases, reaches a maximum at $50 \%$ duty ratio and then decreases
(d) keeps on increasing as the duty ratio increase.
32. If a class-C power amplifier has an input signal with frequency of 200 kHz and the width of collector current pulses of $0.1 \mu \mathrm{~s}$, then the duty cycle of the amplifier will be
(a) $1 \%$
(b) $2 \%$
(c) $10 \%$
(d) $20 \%$
33. In schottky TTL, a Schottky diode is used primarily to
(a) act as a switch
(b) act as a controlling switch
(c) prevent saturation of the transistor
(d) saturate this transistor
34. In 8085 microprocessor, the value of the most significant bit of the result following the execution of any arithmetic or Boolean instruction is stored in the
(a) carry status flag
(b) auxiliary carry status flag
(c) sign status flag
(d) zero status flag
35. If the input to the digital circuit (figure) consisting of a cascade of 20 EX-OR gates is $X$, then the output of Y is equal to

(a) 0
(b) 1
(c) $\overline{\mathrm{X}}$
(d) X
36. In a JK flip-flop we have $\mathrm{J}=\overline{\mathrm{Q}}$ and $\mathrm{K}=1$ (shown in figure). Assuming the flip-flop was initially cleared and then clocked for 6-pulses, the sequence at the Q output will be

(a) 010000
(b) 011001
(c) 010010
(d) 010101
37. The most common modulation system used for telegraphy is
(a) frequency shift keying
(b) two tone modulation
(c) pulse code modulation
(d) single tone modulation
38. The counter starts off in the 0000 state, and then clock pulses are applied. Sometime later the clock pulses are removed and the counter FFs read 0011. How many clock pulses have occurred?
(a) 3
(b) 35
(c) 51
(d) any of them
39. A ROM is used to store the table for multiplication of two 8 -bit unsigned integers
(a) $256 \times 16$
(b) $64 \mathrm{~K} \times 8$
(c) $4 \mathrm{~K} \times 16$
(d) $64 \mathrm{~K} \times 16$
40. The decoding error of the counter can be avoided by
(a) increasing propagation delay of flip-flops used in the counter
(b) using very fast logic
(c) using the strobe signal
(d) reducing the propagation delay of flip-flops used in the counter
41. PWM switching is preferred in voltage source inverters for the purpose of
(a) controlling output voltage
(b) output harmonics
(c) reducing filter size
(d) controlling output voltage, output harmonics and reducing filter size
42. Shifting a register to the left by one bit position is equivalent to (in Binary code)
(a) division by 2
(b) multiplication by 2
(c) addition of 2
(d) subtraction of 2
43. In an FM Stereo multiplex transmission, the
(a) sum signal modulates the 19 KHz subcarrier
(b) different signal modulates the 19 KHz subcarrier
(c) different signal modulates the 38 KHz subcarrier
(d) different signal modulates the 67 KHz subcarrier
44. A Signed integer has stored in a byte using 2 's complement format. We wish to store the same integer in 16-bit word. We should copy the original byte to the less significant byte of the word and fill the more significant byte with
(a) 0
(b) 1
(c) equal to the MSB of the original byte
(d) complement of the MSB of the original byte
45. The data bus in $8080 \mathrm{~A} / 8085$ microprocessor is a group of
(a) eight bidirectional lines that are used to transfer 8 bits between the microprocessor and its I/O and memory.
(b) eight lines used to transfer data among the registers
(c) eight unidirectional lines that are used for I/O devices
(d) sixteen bidirectional lines that are used for data transfer between the microprocessor and memory.
46. A master slave configuration consists of two identical flip-flops connected in such a way that output of the master is input to slave. Which one of the following is correct?
(a) master is level triggered and salve is edge triggered.
(b) master is edge triggered and salve is level triggered.
(c) master is positive edge triggered and slave is negative edge triggered.
(d) master is negative edge triggered and slave is positive edge triggered.
47. In an 8085 microprocessor system with memory mapped I/O
(a) I/O devices have 16-bit addresses.
(b) I/O devices are accessed using IN and OUT instructions
(c) there can be a maximum of 256 input devices and 256 output devices.
(d) arithmetic and logic operations can be directly performed with the I/O data
48. A 3-phase voltage source inverter is operated in $180^{\circ}$ conduction mode. Which one of the following statement is true?
(a) both pole voltage and line voltage will have $3^{\text {rd }}$ harmonics components
(b) pole voltage will have $3^{\text {rd }}$ harmonic component but line voltage will be free from $3^{\text {rd }}$ harmonic
(c) line voltage will have $3^{\text {rd }}$ harmonic component but pole voltage will be free from $3^{\text {rd }}$ harmonic
(d) both pole voltage and line voltage will be free from $3^{\text {rd }}$ harmonic components.
49. 12 MHz clock frequency is applied to a cascaded counter of MOD-3 counter, MOD-4 counter and MOD- 5 counter. What are the lowest output frequency and the overall respectively?
(a) $200 \mathrm{KHz}, 50$
(b) $1 \mathrm{MHz}, 60$
(c) $3 \mathrm{MHz}, 12$
(d) $4 \mathrm{MHz}, 12$
50. Which of the following statements is true?
(a) ROM is a Read/Write memory
(b) PC points to the last instruction that was executed
(c) Stack works on the principle of LIFO
(d) All instructions affect the flags

## SECTION - B (Short answer type question) (100 Marks) <br> All questions carry equal marks of 5 each. <br> This Section should be answered only on the Answer Sheet provided.

1. With the neat diagram explain the class B Push-Pull amplifier?
2. Explain operation of CB configuration with neat circuit diagram and output characteristics of CB mode BJT.
3. Use K -map to minimize the following sop expression $A B C D+A B \bar{C} \bar{D}+A \bar{B} \bar{C} \bar{D}+\bar{A} \bar{B} C D+A \bar{B} C D+\bar{A} \bar{B} C \bar{D}+A B C \bar{D}+A \bar{B} C \bar{D}$
4. Write a program to add ten data bytes. Data is stored in memory locations starting from C 300 H . Result is 16 bit. Store the result from D200H.
5. Explain mono stable Multivibrator using IC555.
6. Draw block diagram of 8253 and setup it as square wave generator with 1 msec period if input frequency 1MHZ.
7. What are the advantages of using a free-wheeling diode in the converter circuit? What is the use of free-wheeling diode with RL load? Explain the change in voltage waveform of a full wave converter due to free-wheeling diode.
8. With the neat diagram explain the working of two-stage RC-coupled amplifier.
9. With neat circuit diagram explain the working principle of single phase semi converter draw its waveforms.
10. Design a 5 minute clock using the 8254 and the interrupt technique.
11. Explain single side band modulation. Explain any one method of generation of SSB waves. Draw neat diagrams wherever necessary.
12. A step up-down (Buck-Boost) chopper has input dc voltage of 220 V and output voltage of 660 V . If the conduction time of the chopper is $120 \mu \mathrm{~s}$, compute the pulse width of the load voltage. In case the pulse width of load voltage is increased to three times its previous width, for constant frequency operation, calculate the new value of average output voltage.
13. Discuss the principle of working of a three phase bridge inverter with an appropriate circuit diagram. Draw phase and line voltage waveforms on the assumption that each thyristor conducts for 120U and the resistive load is star-connected. The sequence of firing of various SCRs should also be indicated in the diagram.
14. Write a delay sub routine to generate a delay of 0.5 sec , if operating frequency of 8085 microprocessor is 3 MHZ .
15. Describe a gate triggering circuit for a single phase full converter. Discuss how the adjustment of control voltage varies the firing delay angle.
16. Explain principle of operation of time ratio control \& current limit control strategies for Chopper circuit.
17. Explain different addressing modes of 8085.
18. What is PWM? What are its advantages? Explain sine pulse width modulation technique.
19. What do you mean by frequency modulation? How many types of F.M. and explain narrow band F.M.?
20. Draw the logic diagram and excitation table of
(a) D-flip flop
(b) J- K flip flop
